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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PETERSON, CHRISTOPHER K

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/728,243	Applicant(s) JUNG, DUCK YOUNG	
	Examiner CHRISTOPHER K. PETERSON	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 May 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-6,15 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-6,15 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

The Amendment After Non-Final Rejection filed on May 21, 2008 has been received and made of record. Examiner notes that the Applicant has added new claim 20, which include limitations similar to those of claims 1 and 15. Claims 1, 4 - 6, 15, and 20 are pending in this application.

Response to Arguments

1. Applicant's arguments filed 5/21/2008 have been fully considered but they are not persuasive.

First in regard to claims 1, 15, and 20, the Applicant has amended the claims to include the limitation of "a photocell which receives light in response to a first shutter control signal". The Applicant argues that Rotzoll discloses a comparator which receives integrated voltage outputs $V1(t)$ and $V2(t)$ from photodiodes 1000 disposed in pixels 420 (FIGS. and 4, 6A, 6B and 7), based on the start of an integration period, and outputs a comparison result directly to a processing means 420 (FIG. 4). More specifically, the device of Rotzoll integrates analog output voltages $V1(t)$ and $V2(t)$ for a predetermined period of time, based on a desired scaling factor K , to subsequently output a signal (corresponding to a detected edge) from the comparator to a processor in response to the end of the integration period. After outputting the signal to the processor, a subsequent integration period starts, at which time voltage outputs $V1(t)$

and $V_2(t)$ are again applied to the comparator. (See, e.g., column 10, line 37 to column 11, line 38 and FIGS. 7 and 8 of Rotzoll) (See Remarks Page 7, lines 1 – 10). The Examiner respectfully disagrees. Specifically, noting the Rotzoll reference, Fig. 6A, 8, and 9 and Col. 8, line 57 – Col.11, line 57 shows that shutter control signal (CSH of application) corresponded with the Φ_2 (Fig. 6A, 7, and 9 of Rotzoll). Rotzoll teaches the comparator circuit (1300A – D) is latched upon activation of a second timing signal Φ_2 (at a time t_2 corresponding to the **end of the integration period**) to provide the output signal representative of the difference between the signals applied on its two inputs. The Applicant contends the Rotzoll creates a subsequent integration period starts, at which time voltage outputs $V_1(t)$ and $V_2(t)$ are again applied to the comparator. Rotzoll teaches that a first integrated signal $V_1(t)$ of a first pixel (pixel) and a second integrated signal $V_2(t)$ of a second pixel (adjacent pixel) may therefore be illustrated as linear curves (Col. 10, lines 21 – 36). Rotzoll further teaches that the integration of the first integrated signal $V_1(t)$ at the end of a first time period $t_1 - t_0$ (this interruption being controlled via the first timing signal Φ_1) results in a voltage signal having a first value $V_1(t_1)$. Continuation of the integration of the second integrated signal $V_2(t)$ until the end of a second time period $t_2 - t_0$, or **integration period, (this being controlled by the second timing signal Φ_2)** results in a voltage signal having a second value $V_2(t_2)$. Similarly, interruption of the integration of the second integrated signal $V_2(t)$ at time t_1 and continuation of the integration of the first integrated signal $V_1(t)$ until time t_2 result in voltage signals having first and second values $V_2(t_1)$ and $V_1(t_2)$ (Col. 10, lines 51 – 67). The first timing signal Φ_1 (V_{out1}) creates the non-scaled images of the integrated

signals of the pixel on the right and the pixel on top are designated by references Vr1 and Vu1 (Col. 9, lines 28 – 43). Therefore when the second timing signal $\Phi 2$ (shutter control signal CSH) is applied to the latch of the comparators (1300A – D), the output of the comparators are latched until the second timing signal $\Phi 2$ (shutter control signal CSH) is activated. For this reason, the Examiner believes that Rotzoll in view of Bock does teach the limitations of the newly amended claims 1, 15, and 20, as set forth in further detail below.

Secondly in regard to claims 1, 15, and 20, the Applicant has amended the claims to include the limitation of “analog signal of a photocell of an adjacent pixel, generates a 1-bit digital signal having a value of the **comparison and maintains the 1-bit digital signal generated by the comparison until a second shutter control signal subsequent to the first shutter control signal is received**”. The Examiner respectfully disagrees. Specifically, noting the Rotzoll reference, Fig. 6A, 8, and 9 and Col. 8, line 57 – Col.11, line 57 shows that shutter control signal (CSH of application) corresponded with the $\Phi 2$ (Fig. 6A, 7, and 9 of Rotzoll). Applicant’s specification does not teach a second shutter control signal. Examiner reads the limitation “a second shutter control signal” as to mean the next image to be captured by the pixel array. The Examiner believes that Rotzoll does teach this limitation because the second timing signal $\Phi 2$ (shutter control signal CSH) will maintain the output to the comparator (1300A – D) until the next pulse of second timing signal $\Phi 2$ (shutter control signal CSH). Explanation to the function of second timing signal $\Phi 2$ (shutter control signal CSH). For this reason, the Examiner believes that Rotzoll in view of Bock does teach the

limitations of the newly amended claims 1, 15, and 20, as set forth in further detail below.

Claim Objections

2. Claims 1, 15, and 20 recite the limitation "a first shutter control signal and a second shutter control signal" in line 3 and 8. There is insufficient antecedent basis for this limitation in the claim. Applicant's specification does not teach a first and second shutter control signal. Examiner will analyze the limitation as a first image capture and second image capture.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1 and 4 - 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotzoll (US Patent 6,806,458) in view of Bock (US Patent 6,707,410).

As to claim 1, Rotzoll (Fig. 6A) teaches an image sensor (photo detector array 420 of Fig. 4) having a plurality of pixels, each pixel comprising:

- a photocell (photosensitive element 1000 and integrating circuit 1100) which receives light in response to a first shutter control signal (second timing signal $\Phi 2$) and generates an analog signal ($V_{out}(t)$) corresponding to a quantity of the received light (Col. 3, line 57 – Col. 4, line 5). Rotzoll shows the pixel in greater

detail in figure 3. The photosensitive element (1000) and the integrating circuit (1100) (support hardware) provide an analog signal ($V_{out}(t)$).

- a latch type comparator (comparator circuit 1300 A-D) which compares the analog signal ($V_{out}(t)$) of the photocell ($V_1(t)$) and an analog signal ($V_{out}(t)$) of a photocell of an adjacent pixel (V_{r1} (pixel on the right) or V_{u1} (pixel on top)), generates a 1-bit digital signal having a value of the comparison and maintains the 1-bit digital signal generated by the comparison (output of 1300B and D) until a second shutter control signal ($\Phi 2$) subsequent to the first shutter control signal ($\Phi 2$) is received. In figure 7, Rotzoll shows the latch type comparator (1300) in greater detail. The timing signal ($\Phi 2$) is used to latch the comparator (Col. 10, lines 46 – 50). Rotzoll also teaches that the **integration period, (this being controlled by the second timing signal $\Phi 2$)** results in a voltage signal having a second value $V_2(t_2)$ (Col. 10, lines 51 – 67). It is well known in the art that a comparator acts like an analog to digital converter; therefore the output (E_x - and E_y -) would either be high or low giving two different outputs.

Rotzoll (Fig. 1) teaches the outputs of the comparators go through a NAND gate (1765, 1770, and 1775) and latch (1760 A-C) (Col. 3, lines 45 – 49). Rotzoll also teaches the NAND gates of figure 2 are not illustrated in figure 6A and B. Rotzoll does not specifically teach a switch. Rotzoll teaches the output may be directly supplies to the processing means (Col. 9, lines 49 – 58). The Bock reference is bought in to teach a switch on the output of the comparator. Bock (Fig. 3) teaches a latch type comparator with a switch (306) on the output of the comparator (Col. 3, lines 61 – 64). Bock

teaches transistor 307 connects a given row to the read-out line 309, which is common for all pixels in a given column and connect to node-C of the digital processing circuit 203 (Col. 3, lines 61 – 64). The comparator is used with additional circuitry to perform analog-to-digital conversion. Replacing the analog-to-digital converter and memory of a conventional digital pixel sensor minimizes many issues associated with conventional digital pixel sensors while preserving the architecture's resistance to noise and speed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a switch as taught by Bock to the sensing device and optical pointing device of Rotzoll, because the digital pixel sensor (DPS) architecture preserves the superior noise, low power consumption, and speed characteristics associated with digital pixel systems (Col. 1, line 54 – Col. 2, line 8).

As to claim 4, Rotzoll wherein the analog signal ($V_{out}(t)$) of the photocell (1000 and 1100) of the adjacent pixel (V_{r1} (pixel on the right) or V_{u1} (pixel on top)) is a reference voltage (Col. 9, lines 28 – 42).

As to claim 5, Rotzoll teaches wherein the photocell (1000 and 1100) is a photo diode (1000) that generates a photocurrent corresponding to the received quantity of light (Col. 8, lines 57 – 65).

As to claim 6, Rotzoll teaches wherein the latch type comparator (1300 A-D) outputs ($Ex-$ and $Ey-$) a first signal when the analog signal ($V_{out}(t)$) of the photocell (1000 and 1100) is greater than the analog signal (V_{r1} or V_{u1}) of the photocell (1000 and 1100) of the adjacent pixel (pixel on the right or pixel on top) and outputs a second signal when the analog signal ($V_{out}(t)$) of the photocell (1000 and 1100) is less than the analog

signal (Vr1 or Vu1) of the photocell (1000 and 1100) of the adjacent pixel (pixel on the right or pixel on top) (Col. 9, lines 28 – 42). It is well known in the art that a comparator acts like an analog to digital converter; therefore the output (Ex- and Ey-) would either be high or low giving two different outputs.

Claims 15 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rotzoll (US Patent 6,806,458) in view of Bock (US Patent 6,707,410) further in view of Arias – Estrada (US Patent 6,253,161).

As to claim 15, Rotzoll an optical pointing system comprising:

a) a plurality of pixels(photo detector array 420) ((Col. 7, lines 32 – 50), each comprising:

- a photocell (photosensitive element 1000 and integrating circuit 1100) which receives light in response to a first shutter control signal (second timing signal $\Phi 2$) and generates an analog signal (Vout(t)) corresponding to a quantity of the received light (Col. 3, line 57 – Col. 4, line 5). Rotzoll shows the pixel in greater detail in figure 3. The photosensitive element (1000) and the integrating circuit (1100) (support hardware) provide an analog signal (Vout (t)).
- a latch type comparator (comparator circuit 1300 A-D) which compares the analog signal (Vout (t)) of the photocell (V1(t)) and an analog signal (Vout (t)) of a photocell of an adjacent pixel (Vr1 (pixel on the right) or Vu1(pixel on top)), generates a 1-bit digital signal having a value of the comparison and maintains the 1-bit digital signal generated by the comparison (output of 1300B and D) until

a second shutter control signal ($\Phi 2$) subsequent to the first shutter control signal ($\Phi 2$) is received. In figure 7, Rotzoll shows the latch type comparator (1300) in greater detail. The timing signal ($\Phi 2$) is used to latch the comparator (Col. 10, lines 46 – 50). Rotzoll also teaches that the **integration period, (this being controlled by the second timing signal $\Phi 2$)** results in a voltage signal having a second value $V2(t2)$ (Col. 10, lines 51 – 67). It is well known in the art that a comparator acts like an analog to digital converter; therefore the output (Ex- and Ey-) would either be high or low giving two different outputs.

Rotzoll (Fig. 1) teaches the outputs of the comparators go through a NAND gate (1765, 1770, and 1775) and latch (1760 A-C) (Col. 3, lines 45 – 49). Rotzoll also teaches the NAND gates of figure 2 are not illustrated in figure 6A and B. Rotzoll does not specifically teach a switch. Rotzoll teaches the output may be directly supplies to the processing means (Col. 9, lines 49 – 58). The Bock reference is bought in to teach a switch on the output of the comparator. Bock (Fig. 3) teaches a latch type comparator with a switch (306) on the output of the comparator (Col. 3, lines 61 – 64). Bock teaches transistor 307 connects a given row to the read-out line 309, which is common for all pixels in a given column and connect to node-C of the digital processing circuit 203 (Col. 3, lines 61 – 64). The comparator is used with additional circuitry to perform analog-to-digital conversion. Replacing the analog-to-digital converter and memory of a conventional digital pixel sensor minimizes many issues associated with conventional digital pixel sensors while preserving the architecture's resistance to noise and speed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

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invention was made to have provided a switch as taught by Bock to the sensing device and optical pointing device of Rotzoll, because the digital pixel sensor (DPS) architecture preserves the superior noise, low power consumption, and speed characteristics associated with digital pixel systems (Col. 1, line 54 – Col. 2, line 8).

b) Rotzoll teaches an image processor (processing means 400) which calculates a movement value based on a plurality of the 1-bit digital signals outputted from the plurality of pixels and generates the pixel select signal and a shutter control information signal based on the movement value (Col. 8, lines 13 – 21). Rotzoll teaches the use of a processing means to calculate a movement value and a shutter control signal ($\Phi 2$). Rotzoll does not specifically teach a pixel select signal. Bock (Fig. 3) teaches a latch type comparator with a switch (306) on the output of the comparator (Col. 3, lines 61 – 64). Bock teaches transistor 307 connects a given row to the read-out line 309, which is common for all pixels in a given column and connect to node-C of the digital processing circuit 203 (Col. 3, lines 61 – 64). Rotzoll in view of Bock do not teach a shutter control circuit. Arias – Estrada teaches a shutter control circuit (external circuitry) for generating a shutter control signal corresponding to the shutter control information signal of the image processor (Col. 9, line 20 - 34). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a shutter control information signal as taught by Arias – Estrada to the sensing device and optical pointing device of Rotzoll in view of Bock, because it will provide one or more of the following advantages: continuous velocity vector field extraction, high density array of pixels, high density array of motion vectors in real-time, real-time

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operation, minimize the use of transistors in analog VLSI susceptible to mismatch and process variation. Minimize the number of analog voltages to bias the a VLSI structures reducing routing complexity, compact three-chip solution to the motion computation paradigm: focal plane sensor, RAM memory, digital interface, potential low-cost fabrication, low power consumption, and robust operation (Col. 2, line 55—Col. 3, line 2)

As to claim 20, Rotzoll an optical pointing system comprising:

a) a plurality of pixels(photo detector array 420) ((Col. 7, lines 32 – 50), each comprising:

- a photocell (photosensitive element 1000 and integrating circuit 1100) which receives light in response to a first shutter control signal (second timing signal $\Phi 2$) and generates an analog signal ($V_{out}(t)$) corresponding to a quantity of the received light (Col. 3, line 57 – Col. 4, line 5). Rotzoll shows the pixel in greater detail in figure 3. The photosensitive element (1000) and the integrating circuit (1100) (support hardware) provide an analog signal ($V_{out}(t)$).
- a latch type comparator (comparator circuit 1300 A-D) which compares the analog signal ($V_{out}(t)$) of the photocell ($V_1(t)$) and an analog signal ($V_{out}(t)$) of a photocell of an adjacent pixel (V_{r1} (pixel on the right) or V_{u1} (pixel on top)), generates a 1-bit digital signal having a value of the comparison and maintains the 1-bit digital signal generated by the comparison (output of 1300B and D) until a second shutter control signal ($\Phi 2$) subsequent to the first shutter control signal ($\Phi 2$) is received. In figure 7, Rotzoll shows the latch type comparator (1300) in greater detail. The timing signal ($\Phi 2$) is used to latch the comparator (Col. 10,

lines 46 – 50). Rotzoll also teaches that the **integration period, (this being controlled by the second timing signal $\Phi 2$)** results in a voltage signal having a second value $V_2(t_2)$ (Col. 10, lines 51 – 67). It is well known in the art that a comparator acts like an analog to digital converter; therefore the output (Ex- and Ey-) would either be high or low giving two different outputs.

Rotzoll (Fig. 1) teaches the outputs of the comparators go through a NAND gate (1765, 1770, and 1775) and latch (1760 A-C) (Col. 3, lines 45 – 49). Rotzoll also teaches the NAND gates of figure 2 are not illustrated in figure 6A and B. Rotzoll does not specifically teach a switch. Rotzoll teaches the output may be directly supplies to the processing means (Col. 9, lines 49 – 58). The Bock reference is brought in to teach a switch on the output of the comparator. Bock (Fig. 3) teaches a latch type comparator with a switch (306) on the output of the comparator (Col. 3, lines 61 – 64). Bock teaches transistor 307 connects a given row to the read-out line 309, which is common for all pixels in a given column and connect to node-C of the digital processing circuit 203 (Col. 3, lines 61 – 64). The comparator is used with additional circuitry to perform analog-to-digital conversion. Replacing the analog-to-digital converter and memory of a conventional digital pixel sensor minimizes many issues associated with conventional digital pixel sensors while preserving the architecture's resistance to noise and speed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a switch as taught by Bock to the sensing device and optical pointing device of Rotzoll, because the digital pixel sensor (DPS)

architecture preserves the superior noise, low power consumption, and speed characteristics associated with digital pixel systems (Col. 1, line 54 – Col. 2, line 8).

b) Rotzoll teaches an image processor (processing means 400) which calculates a movement value based on a plurality of the 1-bit digital signals outputted from the plurality of pixels and generates the pixel select signal and a shutter control information signal based on the movement value (Col. 8, lines 13 – 21). Rotzoll teaches the use of a processing means to calculate a movement value and a shutter control signal ($\Phi 2$). Rotzoll does not specifically teach a pixel select signal. Bock (Fig. 3) teaches a latch type comparator with a switch (306) on the output of the comparator (Col. 3, lines 61 – 64). Bock teaches transistor 307 connects a given row to the read-out line 309, which is common for all pixels in a given column and connect to node-C of the digital processing circuit 203 (Col. 3, lines 61 – 64).

Rotzoll in view of Bock do not teach a shutter control circuit. Arias – Estrada teaches a shutter control circuit (external circuitry) for generating a shutter control signal corresponding to the shutter control information signal of the image processor (Col. 9, line 20 - 34). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a shutter control information signal as taught by Arias – Estrada to the sensing device and optical pointing device of Rotzoll in view of Bock, because it will provide one or more of the following advantages: continuous velocity vector field extraction, high density array of pixels, high density array of motion vectors in real-time, real-time operation, minimize the use of transistors in analog VLSI susceptible to mismatch and process variation. Minimize the number of

analog voltages to bias the a VLSI structures reducing routing complexity, compact three-chip solution to the motion computation paradigm: focal plane sensor, RAM memory, digital interface, potential low-cost fabrication, low power consumption, and robust operation (Col. 2, line 55—Col. 3, line 2)

wherein the at least one of the first shutter control signal and the second shutter control signal comprises a first signal based on a period in which the shutter is turned ($\Phi 2$) on and a second signal based on an initial operation (Reset of the integrating circuit (1100)) of the image processor (Col. 8, lines 57 – 65). Rotzoll teaches that the integrating circuit 1100 may be reset by activation of a RESET signal and released during a determined integration period by deactivation of the RESET signal and as taught above the $\Phi 2$ (shutter control signal) would turn the comparator (1300) on and off.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER K. PETERSON whose telephone number is (571)270-1704. The examiner can normally be reached on Monday - Friday 6:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CKP
6 Aug 2008

***/Ngoc-Yen T. VU/
Supervisory Patent Examiner, Art Unit 2622***